Multiport Register File Design for High-Performance Embedded Cores

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Outline

- Introduction
- Memory design methods
- Simulation results
- Conclusion

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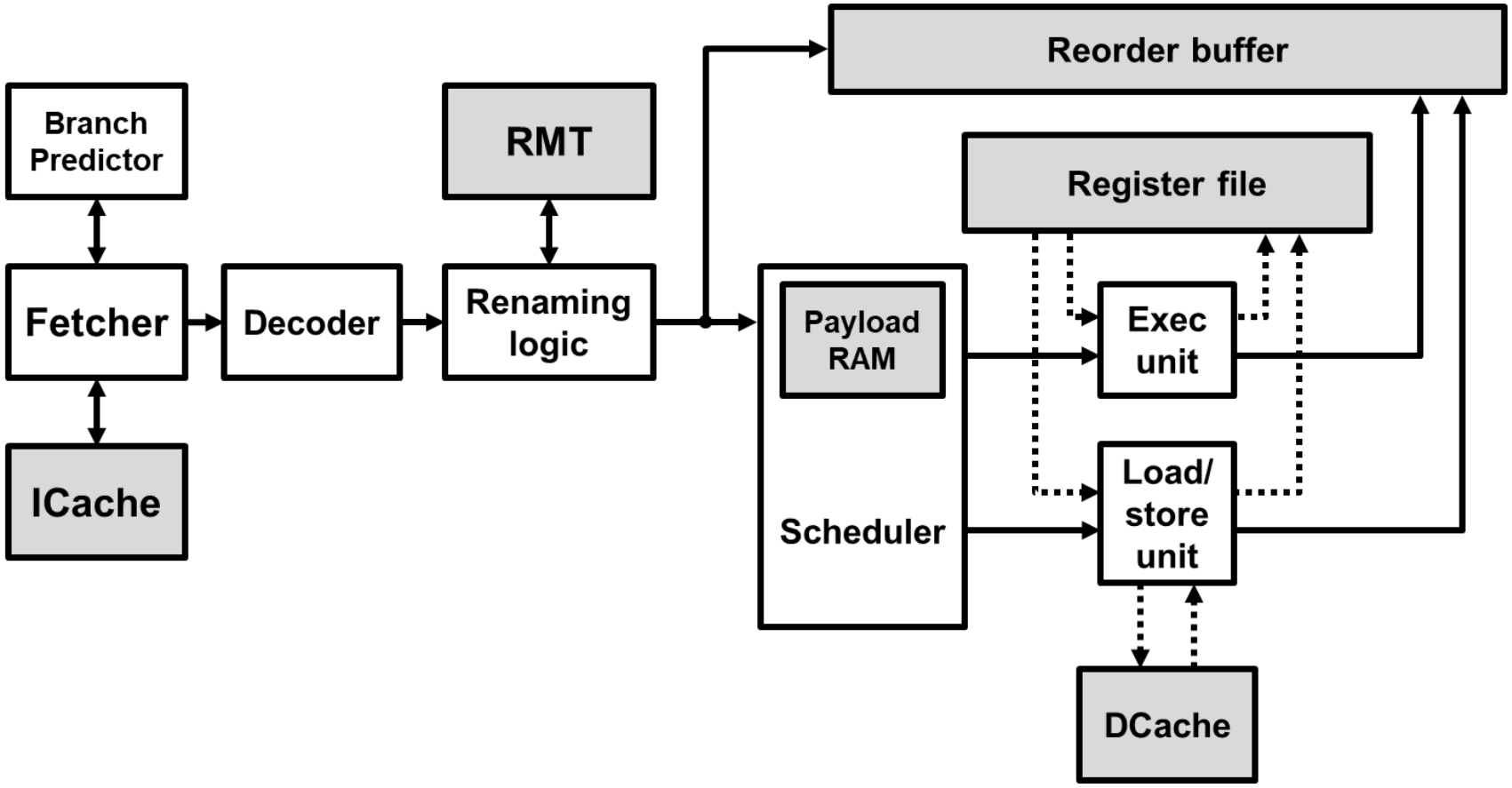
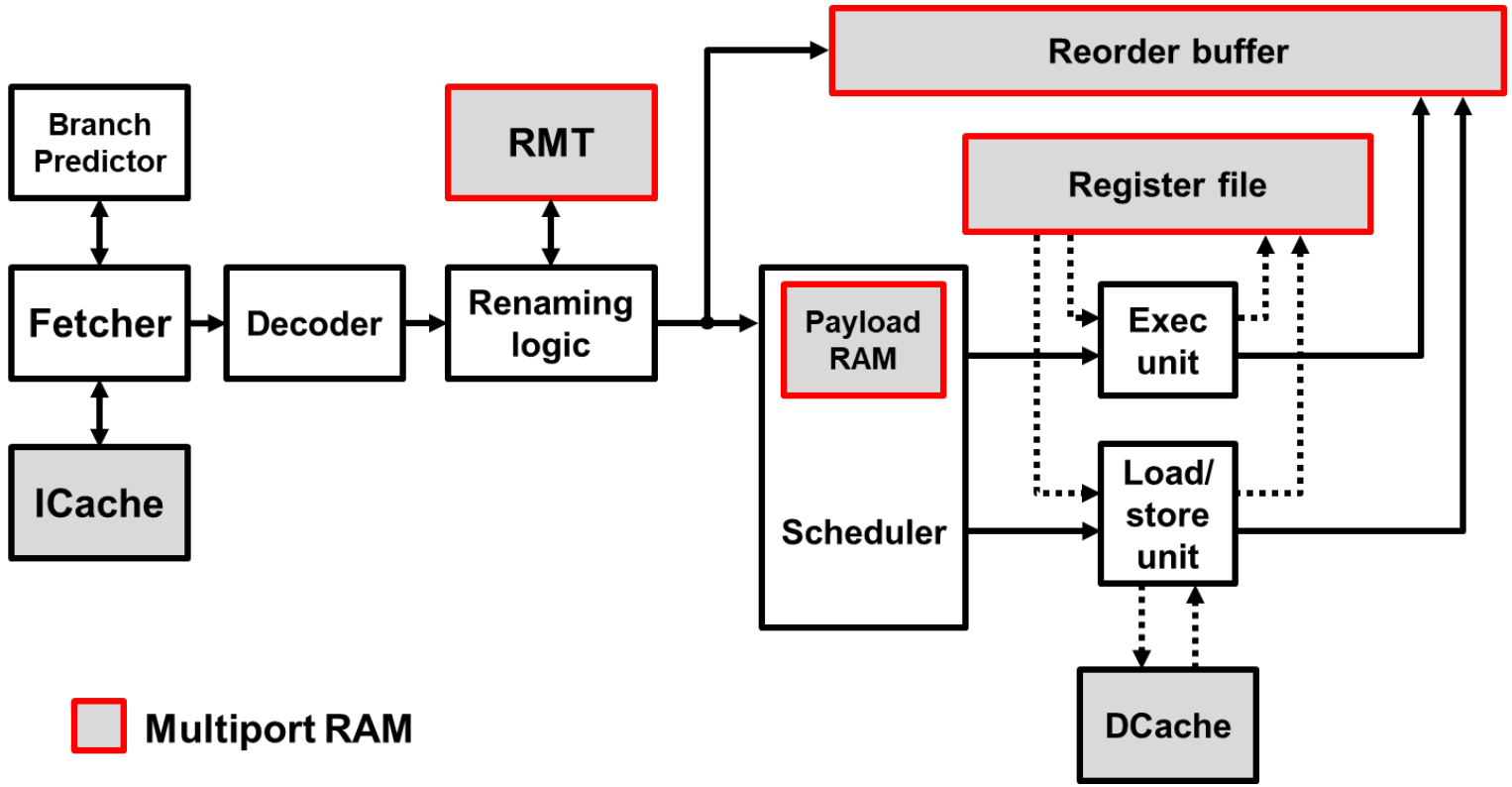
High-Performance Embedded Cores

- Require high single threaded performances
- Out-of-order (OoO) superscalar architectures are widely adopted



Multiport Memories in Superscalar Processor

- I/D cache
- Register map table (RMT)
  - R/W=3*W_{rename}/ W_{rename}
- Scheduler (Payload RAM)
  - R/W=$W_{dispatch}$/ W_{issue}
- Register file
  - R/W=2*W_{issue}/W_{issue}
- Reorder buffer



Challenge for Core Development

- We are currently developing an energy-efficient high-performance 32-bit OoO superscalar processor

- Multiport memory design is one of the most difficult challenges
  - Large area
  - High power consumption

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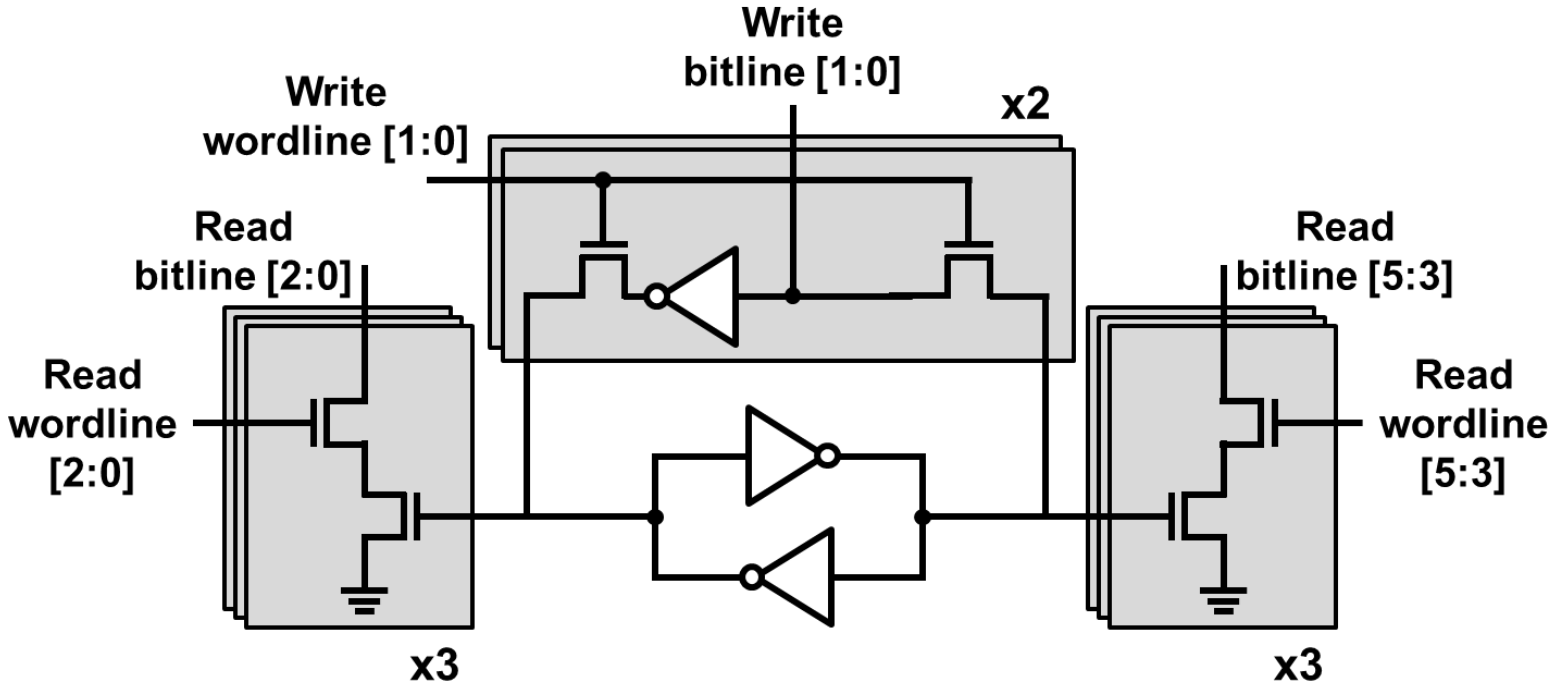
Full-custom SRAM

- Designed from transistors

- Pros
  - High performance
  - Small area
  - Can achieve aggressive scaling of the supply voltage

- Cons
  - Long design time

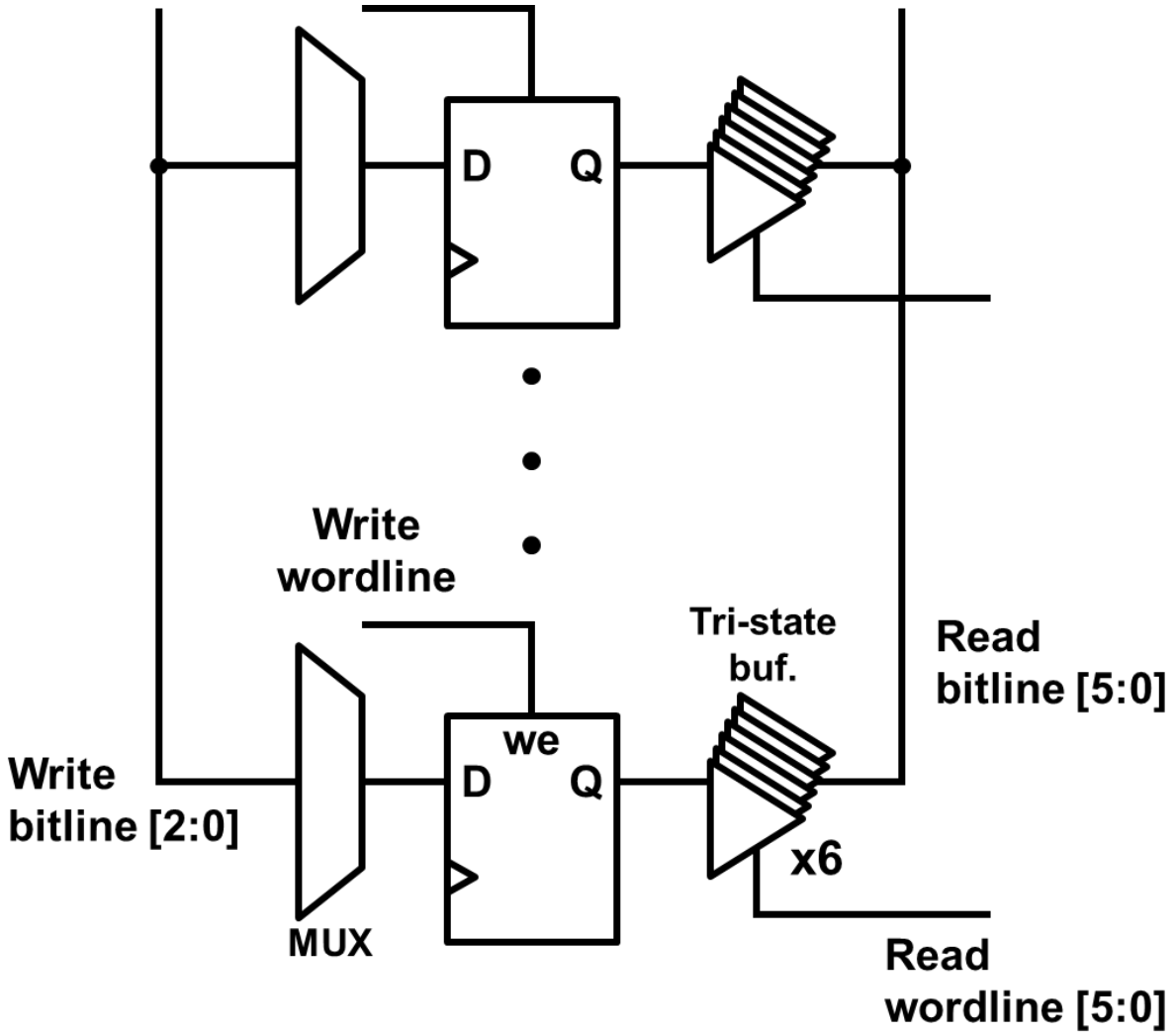


Memory cell of the full-custom designed 6R2W reg. file[1]

[1] J. Warnock, et al., IEEE JSSC, 2006.

Semi-custom SRAM

- Designed from standard-cells
- Pros
  - Achieve aggressive scaling of the supply voltage
- Cons
  - Low performance

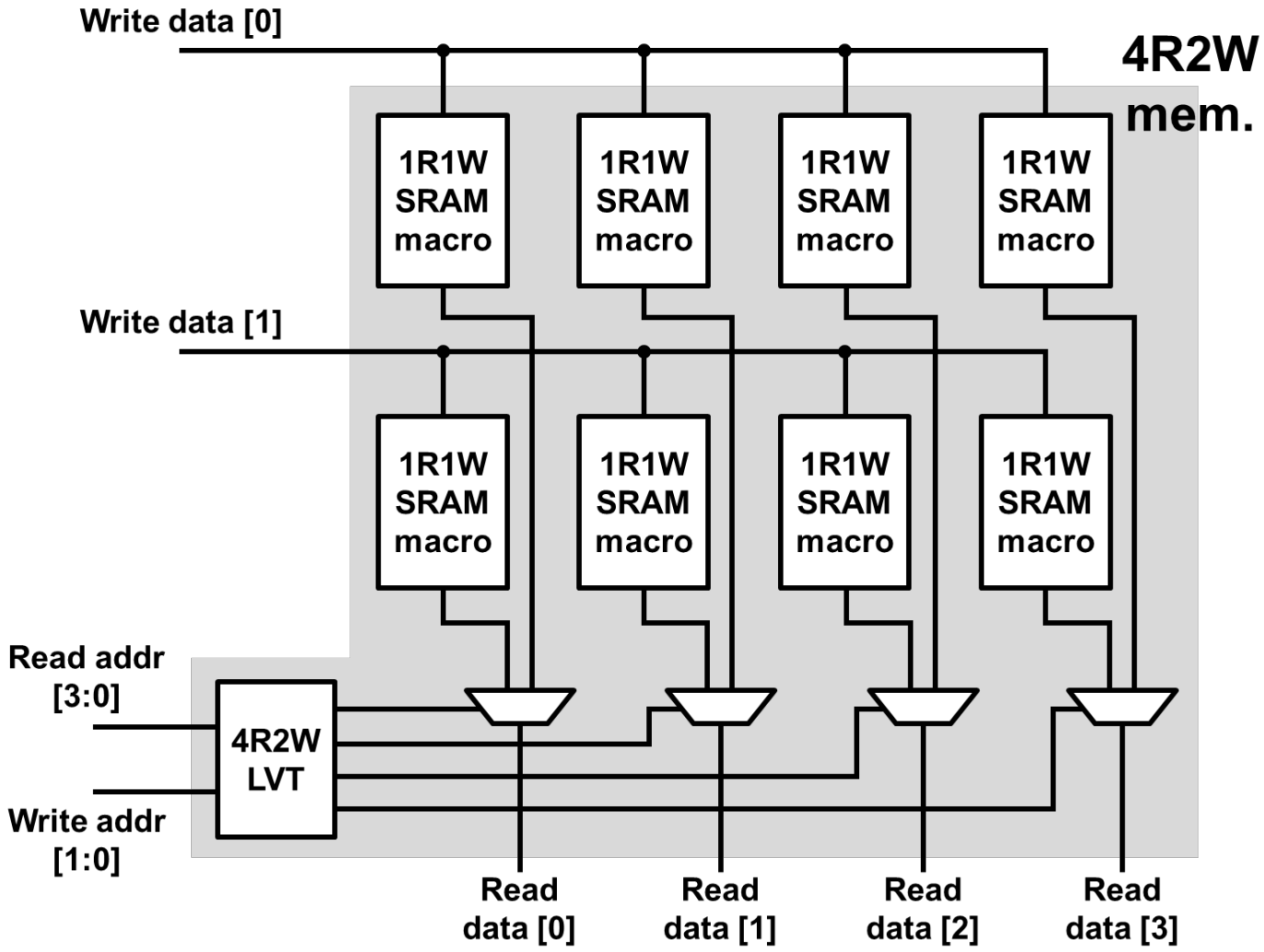


Memory cells of the semi-custom designed 6R3W reg. file[2]

[2] C. Celio, et al., IEEE Micro, 2019.

Algorithmic Multiported Memory (AMM)

- Designed from standard-cells and SRAM macros
- Pros
  - Short design time
- Cons
  - Low performance
  - Large area

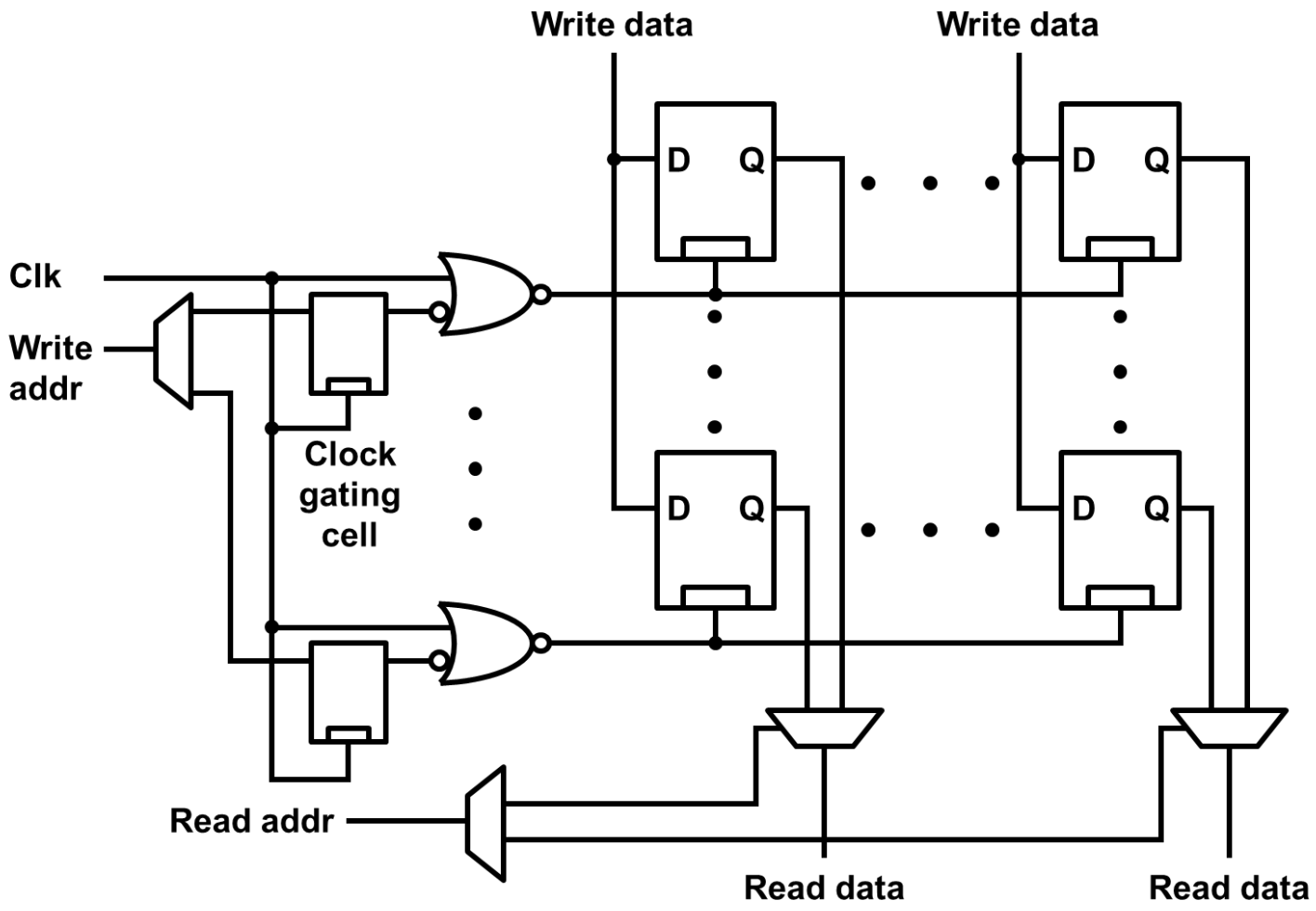


Live value table (LVT) based AMM[3]

[3] C. E. LaForest, et al., ACM/SIGDA FPGA, 2010.

Standard-Cell Based Memory (SCM)

- Designed from standard-cells
- Pros
  - Short design time
  - Achieve aggressive scaling of the supply voltage
- Cons
  - Low performance
  - Large area



D-latch based SCM[4]

[4] O. Anderson, et al., IEEE TCAS-I, 2016.

General Comparison

Method	Performance	Power consumption	Area	Engineering cost	Additional functionality
Full-custom SRAM	H	L	L	H	- Can achieve subthreshold operation
Semi-custom SRAM	L	H	M	M	- Subthreshold operation
Algorithmic multiported memory (AMM)	L	H	H	L	- Easy design reuse
Standard-cell based memory (SCM)	L	H	H	L	- Subthreshold operation - Easy design reuse

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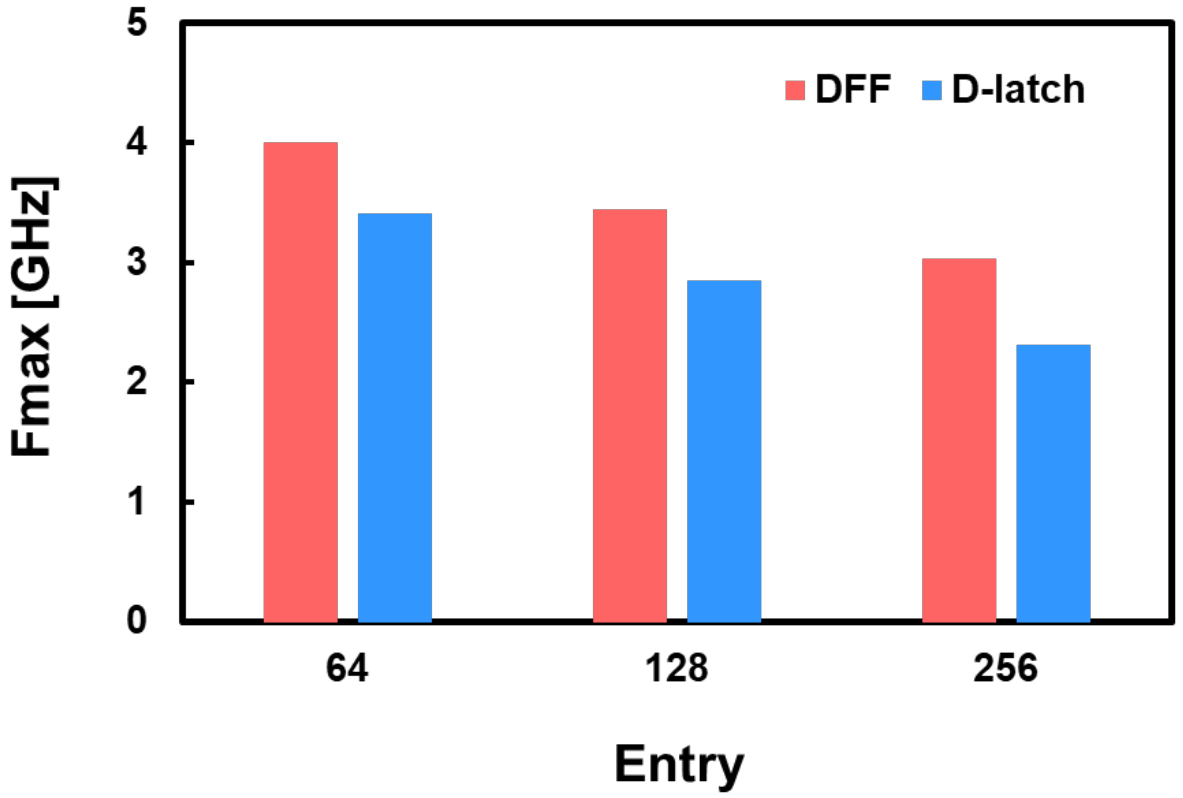
Simulation Results (1/3)

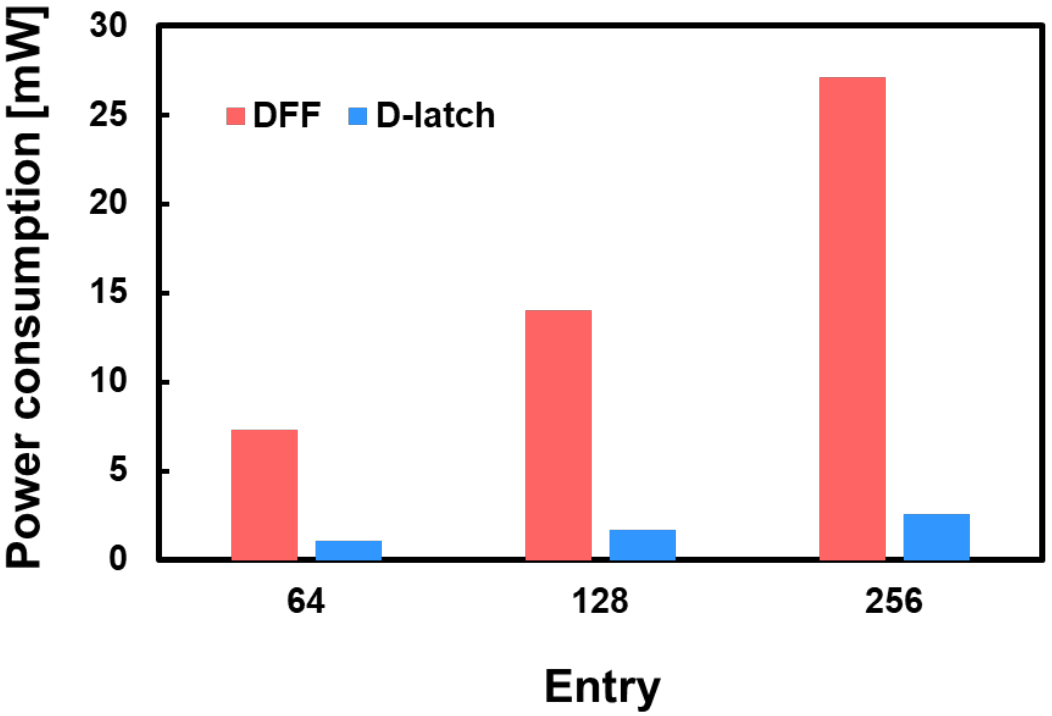
- We designed DFF and D-latch based SCMs in 28-nm CMOS technology

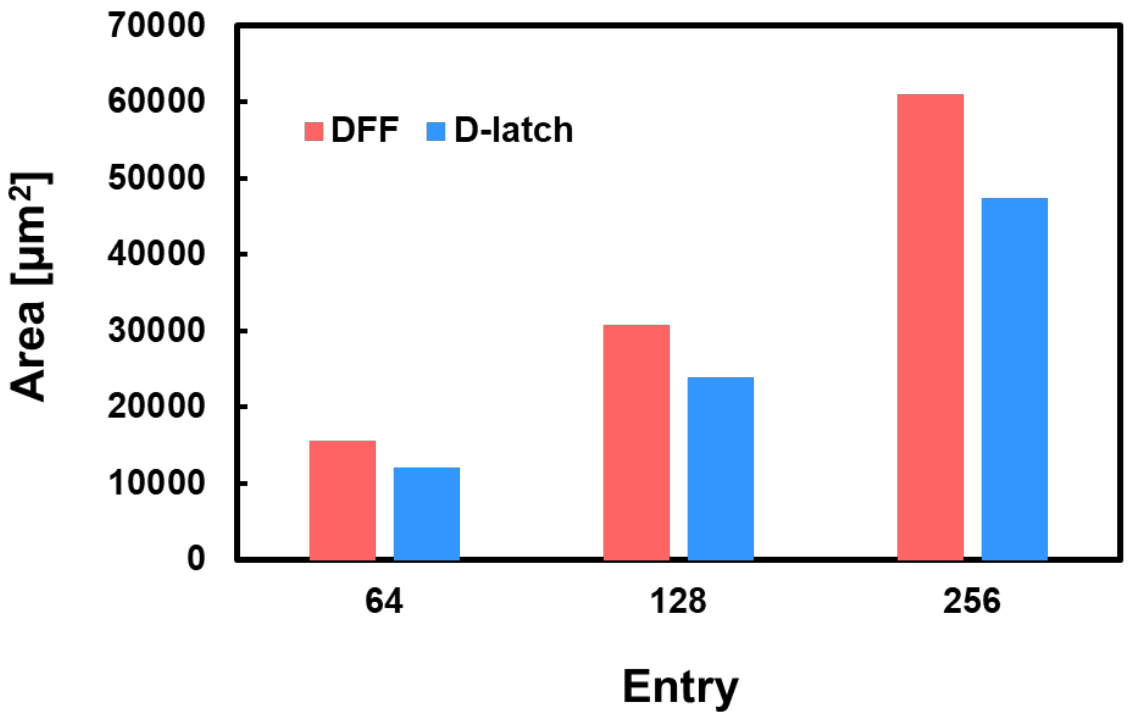
- Maximum operating frequency vs Number of Entries



Simulation Results (2/3)

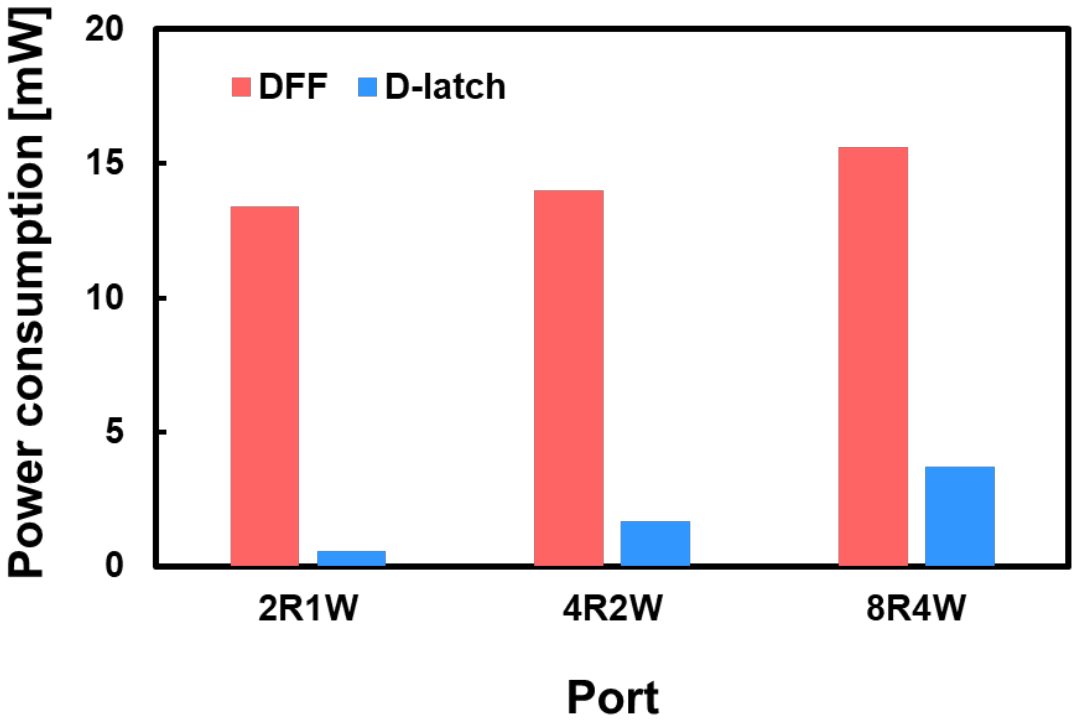
- Power consumption/Area vs Number of Entries

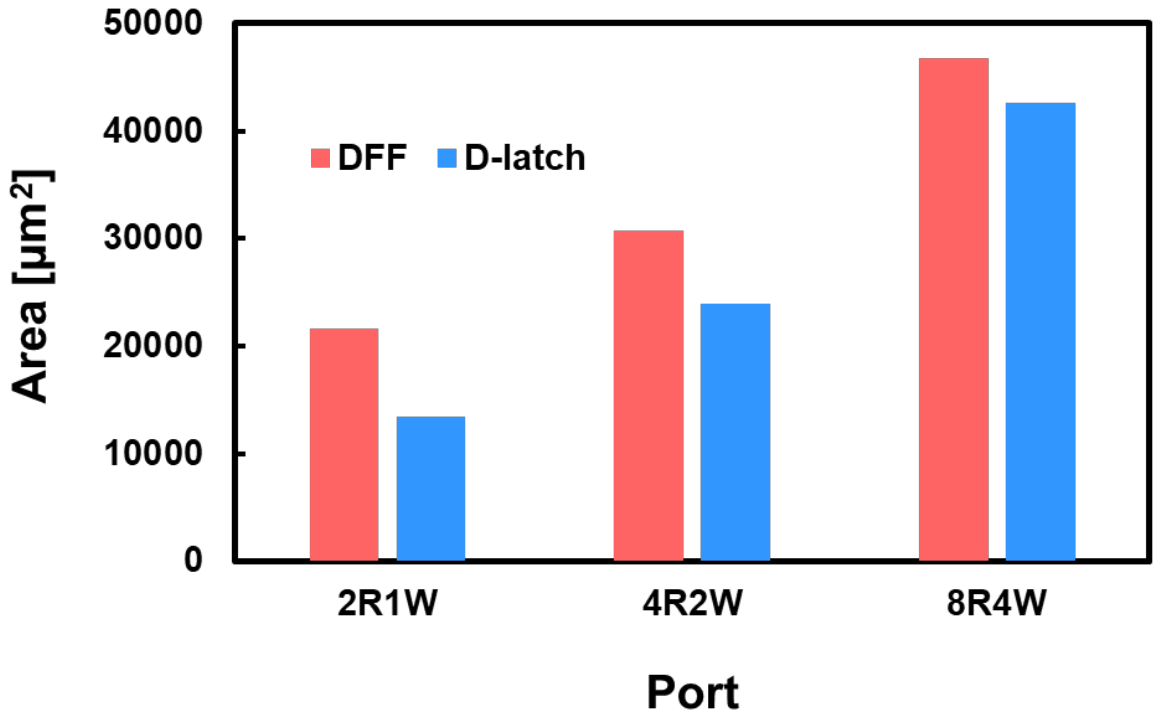




Simulation Results (3/3)

- Power consumption/Area vs Number of Ports





Comparison

- D-latch based SCM can achieve relatively high operating frequency and small area

	D-latch based SCM	LVT based AMM	Full-custom SRAM [5]
Process	28-nm CMOS	28-nm CMOS	28-nm CMOS
Port	4R2W	4R2W	6R4W
Word x Entry	32 x 128	32 x 128	64 x 64
Fmax [GHz]	2.8	1.4	3.2
Area [μm^2]	23980	46031	26600

[5] H. Hsieh, et al., IEEE CICC, 2015.

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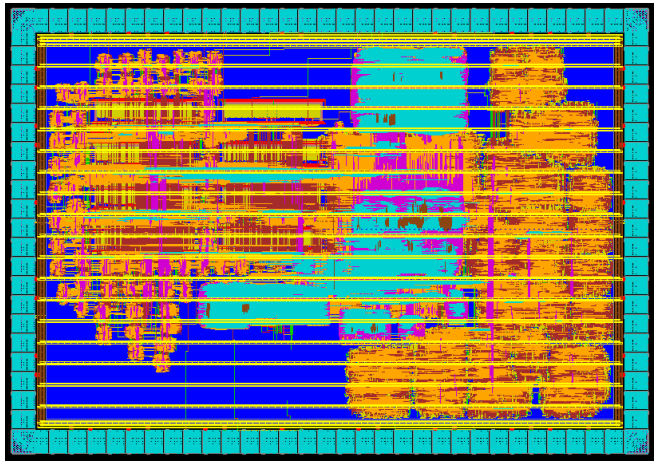
Conclusion

- Multiport memory design methods for superscalar cores
  - Full-custom/semi-custom SRAM, algorithmic multiported memory (AMM), standard-cell based memory (SCM)
  - D-latch based SCM can achieve relatively high operating frequency and small area

- Future work
  - Full-custom SRAM design
  - Test chip development



Initial layout design of the test chip