IEEE MCSoC'13 Final Program

MCSoC'13

2013 IEEE 7th International Symposium on Embedded Multicore/Many-core SoCs

September 26-28 2013

National Institute of Informatics, Tokyo, Japan

Program at a Glance

September 26th			September 27th				September 28th			
9:10	Registration		9:10	Registration			9:10	Registration		
9:30	Opening									
9:50 -10:50	Keynote 1		9:20 -10:20	Keynote 3			9:20 -10:20	Keynote 6		
10:50 -11:05	Coffee break		10:20 -10:35	Coffee break			10:20 -10:35	Coffee break		
11:05 -11:50	ATMG invited 1		10:35 -11:20	LHAM invited 1			10:35 -12:05	McSoC5	McSoC6	Special Session: NEST
11:50 -13:00	Lunch		11:25 -12:40	McSoC3	Special Session: LHAM1	Special Session: HMC				
13:00 -14:40	McSoC1	Special Session: ATMG1	12:40 -13:50	Lunch			12:05 -12.20	Closing		
14:45 -15:45	Keynote 2		13:50 -14:50	Keynote 4						
15:45 -16:30	ATMG invited 2		14:50 -15:35	LHAM invited 2						
16:30- 16:45	Coffee break		15:35 -15:50	Coffee break						
16:45 -18:00	McSoC2	Special Session: ATMG2	15:50 -17:05	McSoC4	Special Session: LHAM2					
18:05 -18:50	ATMG invited 3		17:10 -18:10	Keynote 5						
19:00 --	Welcome Reception		18:30 --	Banquet						

Time Table and Program

Thursday, September 26th

Start	End	Duration	Session (Room)	Details
9:10	9:30	20 min	Registration	
9:30	9:50	20 min	Opening (Conference room 3 and 4)	Welcome and Opening Remarks
9:50	10:50	60 min	Keynote 1 (Conference rooms 3 and 4)	**"The Plural Architecture: Shared Memory Many-cores with Hardware Scheduling"** Ran Ginosar (*EE & CS, Technion, Israel*) Session Chair: Hideharu Amano (*Keio University, Japan*)
10:50	11:05	15 min	Break	
11:05	11:50	45 min	ATMG invited 1 (Conference rooms 3 and 4)	**"Data-Driven Modeling in Auto-Tuning"** Weichung Wang *(*National Taiwan University, Taiwan*)*
11:50	13:00	70 min	Lunch	
13:00	14:40	100 min	MCSoC 1 (Conference room 4)	**<u>Multicore/Many Core Systems</u>** Chair: Hiroki Nakahara (*Kagoshima University, Japan*) **Software Migration for Parallel Execution on a Multicore Tablet: A Case Study,** Weihua Sheng, Philipp Szymanski, Rainer Leupers and Gerd Ascheid *(RWTH Aachen University, Germany)* **A fine-grained dependable optically reconfigurable gate array as a multi-soft-core processor platform,** Retsu Moriwaki and Minoru Watanabe *(Shizuoka University, Japan)* **Design and Implementation of an Efficient and Realistic**

				Cooperative Core Architecture, Tomoyuki Nagatsuka and Kenji Kise *(Tokyo Institute of Technology)* **A formal evaluation of mean-time access latencies for interleaved on-chip shared banked-memory in manycores,** Stephane Louise *(CEA LIST, France)*
13:00	14:40	100 min	Special Session: ATMG 1 (Conference room 3)	**<u>Autotuning systems and tools</u>** **Energy Optimization for Scientific Programs using Auto-tuning Language ppOpen-AT,** Takahiro Katagiri, Cheng Luo, Reiji Suda, Shoichi Hirasawa, and Satoshi Ohshima *(The University of Tokyo, Japan)* **BOAST: Bringing Optimization through Automatic Source-to-Source Transformations,** Brice Videau, Vania Marangozova-Martin, and Johan Cronsioe *(LIG, France)* **Auto-Tuning of Data Communication on Heterogeneous Systems**, Marc Jorda (1*), Ivan Tanasic, Javier Cabezas, Lluís Vilanova, Isaac Gelado, and Nacho Navarro *(Barcelona Supercomputing Center)*
14:45	15:45	60 min	Keynote 2 (Conference rooms 3 and 4)	**"Many-core System Designs through Effective Routing Support and Reconfigurability"** José Flich (*Universidad Politécnica de Valencia, Spain*) Session chair: Tsutomu Yoshinaga (The University of Electro-Communications, Japan)
15:45	16:30	45 min	ATMG invited 2 (Conference rooms 3 and 4)	**"Parameter Tuning for Massively Parallel Monte-Carlo Tree Search"** Kazuki Yoshizoe *(Japan Science and Technology Agency / Tokyo Institute of Technology, Japan)*
16:30	16:45	15 min	Break	
16:45	18:00	75 min	MCSoC 2 (Conference room 4)	**<u>NoC Architectures</u>** Chair: Tsutomu Yoshinaga (*The University of Electro-Communications, Japan)*

				Performance Degradation by Deactivated Cores in 2-D Mesh NoCs Ikki Fujiwara, Michihiro Koibuchi and Hiroki Matsutani *(National Institute of Informatics, Japan)* **Design of a GALS-NoC using Soft-cores on FPGAs** Hideki Katabami, Hiroshi Saito *(The University of Aizu, Japan)*) and Yoneda Tomohiro *(National Institute of Informatics, Japan)* **Study of Application of Network Coding on NoCs for Multicast Communications**, Ahmed Shalaby, Mohamed Ragab and Victor Goulart *(Egypt-Japan University of Science and Technology, Egypt)*
16:45	18:00	75 min	Special Session: ATMG 2 (Conference room 3)	**<u>Applications and Performance Evaluation</u>** **OpenMP/MPI Implementation of Tile QR Factorization on T2K open supercomputer,** Tomohiro Suzuki and Hideki Miyashita *(University of Yamanashi, Japan)* **A Comparison of Performance Tunabilities between OpenCL and OpenACC,** Makoto Sugawara(*1), Shoichi Hirasawa, Kazuhiko Komatsu, Hiroyuki Takizawa and Hiroaki Kobayashi *(Tohoku University, Japan)* **Early Experiences for Adaptation of Auto-tuning by ppOpen-AT To Explicit Method,** Takahiro Katagiri, Satoshi Ito and Satoshi Ohshima *(The University of Tokyo, Japan)*
18:05	18:50	45 min	ATMG invited 3 (Conference rooms 3 and 4)	**Verified Numerical Computations for Matrix Multiplication based on High Performance BLAS**, Katsuhisa Ozaki *(Shibaura Institute of Technology, Japan)*
19:00	--	--	Welcome Reception	

Friday, September 27th

Start	End	Duration	Session (Room)	Details
9:10	9:20	10 min	Registration	
9:20	10:20	60 min	Keynote 3 (Conference rooms 3 and 4)	**"Practical Advances and Applications of Asynchronous Design"** Peter A. Beerel *(University of Southern California, U.S.A)* Session chair: Tomohiro Yoneda *(National Institute of Informatics, Japan)*
10:20	10:35	15 min	Break	
10:35	11:20	45 min	LHAM invited1 (Conference rooms 3 and 4)	**"Ease of Porting Parallel HPC Codes to Intel Xeon Phi"** Michael McCool (*Intel, USA*)
11:25	12:40	75 min	MCSoC 3 (Conference room 4)	**<u>Network/Streaming Processing</u>** Chair: Hideyuki Kawashima *(University of Tsukuba, Japan)* **A Packet Classifier using Parallel EVMDD(k) Machine,** Hiroki Nakahara, Tsutomu Sasao and Munehiro Matsuura *(Kagoshima University, Japan)* **A Low-Power Link Speed Control Method on Distributed Real-time Systems,** Yusuke Kumura, Kazutoshi Suito, Hiroki Matsutani and Nobuyuki Yamasaki *(Keio University, Japan)* **Wire-Speed Implementation of Sliding-Window Aggregate Operator over Out-of-Order Data Streams,** Yasin Oge, Masato Yoshimi, Takefumi Miyoshi, Hideyuki Kawashima, Hidetsugu Irie, and TsutomuYoshinaga *(The University of Electro-Communications, Japan)*
11:25	12:40	75 min	Special Session: LHAM 1 (Conference room 3)	**Towards an Extensive Programming Environment for Software Evolution,** Hiroyuki Takizawa *(Tohoku University, Japan)* **Experience of Implementing Parallel FFTs on GPU Clusters,** Daisuke Takahashi *(University of Tsukuba, Japan)*

11:25	12:40	75 min	Special Session: HMC (Conference room 2)	**Reconfigurable Multi-core Architecture - A Plausible Solution to the von Neumann Performance Bottleneck** Chun-Hsien Lu, Chih-Sheng Lin, Hung-Lin Chao, Jih-Sheng Shen, and Pao-Ann Hsiung (National Chung Cheng University, Taiwan) **Performance Evaluation of Cauchy Reed-Solomon Coding on Multicore Systems**, Lars Lundberg and Tim Karlsson *(Blekinge Institute of Technology, Sweden)* **GPU-based Multi-stream Analyzer on Application Layer for Service-oriented Router**, Kazumasa Ikeuchi, Janaka Wijekoon, Shinichi Ishida and Hiroaki Nishi *(Keio University, Japan)*
12:40	13:50	70 min	Lunch	
13:50	14:50	60 min	Keynote 4 (Conference rooms 3 and 4)	**"Network-on-Chip Benchmarks Based on Real MPSoC Applications"** Jiang Xu (*Hong Kong University of Science and Technology, Hong Kong SAR*) Session chair: Kenji Kise (*Tokyo Institute of Technology, Japan*)
14:50	15:35	45 min	LHAM invited 2 (Conference rooms 3 and 4)	**"Software Engineering of Scientific Applications for Portability, Evolvability, and Performance"** Shirley Moore *(The University of Texas at El Paso, USA)*
15:35	15:50	15 min	Break	
15:50	17:05	75 min	MCSoC 4 (Conference room 4)	**<u>NoC Techniques</u>** Chair: Jiang Xu (*Hong Kong University of Science and Technology, Hong Kong SAR*) **"Evaluation of The Scalability of Round Robin Arbiters for NoC Routers on FPGA"** Maher Abdelrasoul, Victor Goulart and M. El-Sayed Ragab *(Egypt-Japan University of Science and Technology, Egypt)* **"Deadlock-Recovery Support for Fault-tolerant Routing**

				Algorithms in 3D-NoC Architectures" Akram Ben Ahmed, Achraf Ben Ahmed, Abderazek Ben Abdallah *(The University of Aizu, Japan)* **Mapping Non-trivial Network Topologies onto Chips,** Ikki Fujiwara and Michihiro Koibuchi *(National Institute of Informatics, Japan)*
15:50	17:05	75 min	Special Session: LHAM 2 (Conference room 3)	**"The Future of Accelerator Programming: Abstraction, Performance or Can We Have Both?**" Kamil Rocki *(The University of Tokyo, Japan)* **"A HPC Refactoring Catalog: Guidelines to Bridge The Gap between HPC System"** Ryusuke Egawa *(Tohoku University, Japan)*
17:10	18:10	60 min	Keynote 5 (Conference rooms 3 and 4)	**"Taming Big Data Streams"** Hideyuki Kawashima (*University of Tsukuba, Japan*) Session chair: Michihiro Koibuchi (*National Institute of Informatics, Japan*)
18:30	--	--	Banquet	

Saturday, September 28th

Start	End	Duration	Session (Room)	Details
9:10	9:20	10 min	Registration	
9:20	10:20	60 min	Keynote 6 (Conference rooms 3 and 4)	**"Embedded and Mobile Software Development for Intel SoCs"** Michael McCool (*Intel, USA*) Session chair: Shinpei Kato (*Nagoya University, Japan*)
10:20	10:35	15 min	Break	
10:35	12:05	90 min	MCSoC 5 (Conference room 4)	**Reconfigurable Computing** Chair: Minoru Watanabe (*Shizuoka University, Japan*) **The Approximate String Matching on the Hierarchical Memory Machine with Performance Evaluation,** Duhu Man, Koji Nakano and Yasuaki Ito *(Hiroshima University, Japan)*

				An Efficient Implementation of the Hough Transform using DSP slices and block RAMs on the FPGA, Xin Zhou, Yasuaki Ito and Koji Nakano *(Hiroshima University, Japan)* **A Classification Processor for a Support Vector Machine with embedded DSP slices and block RAMs in the FPGA,** Yuki Ago, Koji Nakano and Yasuaki Ito *(Hiroshima University, Japan)* (**Short**) **Spatiotemporal circuit design toward efficient reconfigurable SoCs,** Kei Kinoshita, Tomoyuki Okamura, Daisuke Takano, Tetsuhiko Yao and Yoshiki Yamaguchi *(University of Tsukuba, Japan)*
10:35	12:05	90 min	MCSoC 6 (Conference room 3)	**<u>Programming/Design Tool</u>** Chair: Hiroaki Nishi (*Keio University, Japan*) **Solving SAT-encoded Formal Verification Problems on SoC based on a WSAT algorithm with a new Heuristic for Hardware Acceleration,** Kenji Kanazawa and Tsutomu Maruyama *(University of Tsukuba, Japan)* **ArchHDL: A New Hardware Description Language for High-Speed Architectural Evaluation**, Shimpei Sato and Kenji Kise *(Tokyo Institute of Technology, Japan)* **Design, Implementation and evaluation of Built-in Functions on Parallel Programming Model in SMYLE OpenCL,** Noriko Etani, Takuji Hieda and Hiroyuki Tomiyama *(Ritsumeikan University)* (**Short**) **Trace Management and Analysis for Embedded Systems,** Generoso Pagano, Damien Dosimont, Guillaume Huard, Vania Marangozova-Martin and Jean-Marc Vincent *(INRIA, France)*
10:35	12:05	90 min	Special Session: NEST	**<u>Networked Embedded Systems for Internet of Things</u>** **DDNM: Monitoring Environment Noise using Smart Phones,**

			(Conference room 2)	Hong Yao, Guang Yang, Changkai Zhang, Chengyu Hu and Qingzhong Liang *(China University of Geosciences, China)* **Study on influences analysis of RFID and application in Midget Coil Warehouse,** Qingzhong Liang, Yuanyuan Fan and Hong Yao *(China University of Geosciences, China)* **Vulnerability Localization Method Based on Software Structural Signature of Complex Network**, Fan Yang, Huanguo Zhang and Jianming Fu *(Wuhan University, China)*
12:05	12.20	15 min	Closing	